Page 5, replace the third full paragraph (lines 19-25) as follows:

However such etching time control is disadvantageous in the reproducibility deteriorates due to fluctuation in etching conditions and thickness of the cladding layer from wafer to wafer. In order to overcome this problem, there has been proposed a structure in which an etching stop layer 26 as shown in Figure 3. The structure in Figure 3 has an n-side electrode 31, an n-GaAs substrate 21, an n-GaAs buffer layer 22, an n-AlGaAs cladding layer 23, an undoped SCH active layer 24, a p-AlGaAs cladding layer 25, a p-InGaP etching stop layer 26, a p-AlGaAs cladding layer 25, a p-GaAs capping layer 28, a SiO_2 insulating film 29, and a p-side electrode 30. See United States Patent No. 4,567,060 (reference 4).

Pages 5-6, replace the paragraph bridging these pages (p. 5, line 26 to p. 6, line 6) as follows:

For example, in the case where an AlGaAs cladding layer 23/25 and an InGaAsP active region 24 are combined, by inserting an InGaP etching stop layer 26 (about 1 to 5nm in thickness), which is lattice-matched with the GaAs substrate 21, into the upper cladding layer 27 as shown in Figure 3, it becomes feasible to stop etching of the AlGaAs 27 at the InGaP etching stop layer 26 in various etching methods.

Page 13, second full paragraph (lines 7-9) as follows:

Figure 13 is a view showing a comparison of measured relation between the number of quantum wells and the slope efficiency and theoretical relation of the same,

IN THE CLAIMS:

Please add the following new claims:

4. (New) A method of manufacturing a semiconductor laser further to Claim 3, wherein no intermediate layer is formed between the upper optical waveguide layer and the upper cladding layer to protect the upper optical waveguide during said step of selectively removing by etching a part of the upper cladding layer.